09/786787 Rec'd PCT/PTO 09 MAR 2001

FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 2654-005US

U S APPLICATION NO (IF KNOWN, SEE 37 CFR): 09/786787

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/US99/20418	07 September 1999	10 September 1998

TITLE OF INVENTION: **NON-CIRCULAR MICRO-VIA**

APPLICANT(S) FOR DO/EO/US: **COTTON, Martin A.**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U S C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C 371 (c) (2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U S.C 371(c)(3))
10. ☐ An oath or declaration of the inventor(s) (35 U.S C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409)
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Check in the amount of $898.00 ($130 - Declaration filed after 30 months from priority date; $100 - Claims meet PCT Article 33(1)-(4); $560 - 7 extra independent claims; $108 - 6 extra claims (over 20))

U.S. APPLICATION NO (IF KNOWN, SEE 37 CFR) 09/786787	INTERNATIONAL APPLICATION NO PCT/US99/20418	ATTORNEY'S DOCKET NUMBER 2654-005US

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21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1 482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO . .	$1,000.00	
☐	International preliminary examination fee (37 CFR 1 482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	$860.00	
☐	International preliminary examination fee (37 CFR 1 482) not paid to USPTO but international search fee (37 CFR 1 445(a)(2)) paid to USPTO . .	$710.00	
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$690.00	
☒	International preliminary examination fee paid to USPTO (37 CFR 1 482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00	

ENTER APPROPRIATE BASIC FEE AMOUNT =	**$100.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1 492 (e)).	**$130.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	26 - 20 =	6	x $18 00	**$108.00**	
Independent claims	10 - 3 =	7	x $80.00	**$560.00**	
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**	

TOTAL OF ABOVE CALCULATIONS =	**$898.00**	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1 28) **(check if applicable).** ☐	**$0.00**	
SUBTOTAL =	**$898.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)) +	**$0.00**	
TOTAL NATIONAL FEE =	**$898.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3 28, 3.31) **(check if applicable).** ☐	**$0.00**	
TOTAL FEES ENCLOSED =	**$898.00**	
	Amount to be: refunded	$
	charged	$

☒ A check in the amount of **$898.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No **18-1579** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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3-9-2001
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09/786787
JC02 Rec'd PCT/PTO 09 MAR 2001

CERTIFICATE OF EXPRESS MAILING

Express Mail Mailing Label Number EL 765897657 US

Date of Deposit: March 9, 2001

I hereby certify that the Filing under 35 U.S.C. 371 of Martin A. Cotton for **NON-CIRCULAR MICRO-VIA** including the International Application Published Under the PCT; International Search Report; International Preliminary Examination Report; and a check in the amount of $898.00, are being deposited with the United States Postal Service for "Express Mail" service under 37 C.F.R. § 1.10 on the date indicated above and are addressed to the Assistant Commissioner for Patents, Box PCT, Washington, D.C. 20231.

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Non-Circular Micro-Via

Technical Field

This invention relates to Printed Circuit Boards (PCBs) and particularly to micro-via plated through hole interconnect and shielding structures for PCBs and the method for creating such micro-vias and shielding structures.

Background Art

It is always the goal in PCB design to increase the functionality and component capacity. Almost since the inception of PCB's, engineers have striven to add more and more functionality and hence more interconnect traces. These traces go from side to side and from layer to layer and in this way form the interconnect between the "active" electronic elements. The PCB has throughout its lifetime been made from many alternate materials and processes. The most common material being a glass epoxy based laminate, with the PCB builds being of a single sided, double sided or a multilayered (more than 2 layers) configuration. The interconnect medium between layers are created by drilling with mechanical drill through the layers of the PCB exposing the copper interconnect lands on the individual layers. The PCB is then passed through a plating solution and the various layers are connected

by plated or deposited copper formed on the interior surface of the drilled through hole. This drilled plated barrel of inter layer interconnect is called a "via". The most obvious physical attribute is that the via is round when viewed from the top or bottom side. This is caused by "drilling". Drilling holes through laminate causes a round or circular hole to be created. Drilling of holes is carried out on a drilling machine that drills using a "drill", a mechanical device that rotates or cuts around its centerline cutting away material about the centerline to create the round or circular holes. The action of a drill is one of cutting.

As mentioned previously more and more interconnect traces have been required as circuit and hence PCB complexity increased. This of course has led to a decrease in size of the vias and an increase in their number. The new smaller vias are called "micro vias" and are typically of a blind nature. Blind vias are vias that do not pass completely through the PCB, but stop at some predetermined layer depth. The smaller via size is required due to an increase in trace density which reduces the points on a given layer where a terminal interconnect land can be positioned such that it aligns with a land on another layer without interference with traces there between. If cross-sectional real estate that a via occupies is reduced, the ability to utilize a via is more likely. However, the decrease in via size has meant that the mechanical drilling of micro vias is almost commercially extinct. Several alternate processes have sprung up namely laser ablation and plasma ablation. Material ablation is an

electrochemical reaction to either laser light pulsing or the plasma process. It is not a cutting action or process. However, ablation in like manner removes away material around a centerline.

Ablation emulates mechanical drilling by creating a basically circular hole whichever method is used. This ablated round hole is often described as "drilling" because of removal of material about a centerline, hence the term, Micro via drilling. This round hole has performance level based around the creation of a round or circular shape hole, namely, current carrying capacity, resistance and inductance. For example, a blind via has a lower inductance than a through hole because it has shorter length to the barrel of the via, but its current carrying capacity does not alter because the diameter and hence the circumference of the hole remains the same. Therefore, the current carrying capacity of a via is dependent on the circumferencial length and the conducting medium thickness at the point of interconnection between the trace land and the via.

There are several problems with the conventional circular profile micro-via. For example, when densely populated multi-layer PCBs are utilized there are an enormous amount of traces and interconnects. Circular vias may be a limiting feature if the via is to avoid traces or components when extending through multiple layers because of the cutting area required for a circular hole. Also, the current carrying capacity of circular vias are limited because current

carrying capacity of a via is a factor of circumference and thickness of the plating applied to the inner wall. This factor also effects the ability to have multiple traces on a single layer to connect up to the same via because the distance between the contact points are too short thus exceeding the current carrying capacity of the via at those points or the interconnect density at a given land or PCB layer. Conventional standard circular profile micro vias also have a characteristic inductance property due to the spiral nature of the circular via which effects the electron flow through the via resulting in an inductance. The inductance characteristic tends to slow down signal speed and increase noise susceptibility.

Through holes that can possibly be categorized as a Micro-via have been utilized on non-organic silicone based semi-conductor devices to connect two conductive layers separated by an insulation layer where the insulation layer has a contact through hole which exposes a portion of the two conductive surfaces. This through hole embodiment is where one conductive layer continuously extends down through the through-hole thereby electrically connecting the two layers. The semi-conductor via technology has a different purpose and hence a different structure, however it is worth mentioning when discussing via technology (electrical interconnection utilizing a through hole) for completeness. With a semiconductor via the first conductive layer actually conforms to the walls of the through hole and continues over the exposed area of the second layer and in continuous contact with said second layer forming

what may be described as a blind via. However the process of forming the via is different from a process where material is cut away about a centerline and there is no plating structure.

In this semi-conductor example the through-hole is filled with a continuation of a first conductive layer of the semi-conductor into the through hole. The through hole structure utilized for semiconductor designs differs from through holes or micro vias utilized for printed circuit boards. First, micro vias for printed circuit boards interconnect a plurality of circuit trace terminal lands or pads by transcending through and exposing them to an interior conductive plating, whereas the semiconductor through hole structure is that of a hole through an insulation layer that separates two layers of conductive media. The interconnection is established by continuously extending one conductive media layer through the through hole establishing contact with the second layer. Establishing a plurality of interconnections to a node created by a via is not the objective in the semiconductor environment as it is with printed circuit board vias.

The specific issue with regard to semi conductor vias is electrical failure of the via structure due to thermal and other stresses particularly in the area around the rim of the opening of the through hole. This is where the conductive media layer begins to extend through the through hole and failures occur because it is at this point that the media layer tends to be thinner. The

problem is concentration of stresses in a small area. Whereas, with printed circuit boards the issue with vias is the density of the interconnections as it relates to current carrying capacity and better voltage drop.

Disclosure of the Invention

It is in view of the above problems that the present invention was developed.

The invention thus has as an object to provide additional current carrying capacity for a via and reduce its inductance characteristic. It is also object of this invention to provide vias that can physically avoid traces and components for densely populated multiple trace multi-layer boards. It is also an object of this invention to connect traces on two or more layers that are not vertically in line. It is also the object of this invention to reduce inductance of the via.

The invention satisfies the above objects by providing a non-circular via and a method for cutting away material about a centerline for a non-circular via for PCBs. The method of drilling the non-circular via will be by cutting or removing material away about a centerline with a process such as laser ablation or plasma ablation. This type of cutting away of material about a centerline is sometimes referred to as ablation of material as noted above and

allows lateral movement to effect noncircular patterns. This invention utilizes this noncircular approach in three forms, convoluted circle or a square, an extended elongated via up to three times the diameter in depth and a trenched via. The convoluted circle or non-circular via is a Profile Power Micro-via. The Profile via has any shape other than round or circular to create an increased length in circumference over a round or circular format. The Profile via can have a non-circular wave form shape centered on the circumference or pitch circle diameter or an irregular shape that is not based on the round or circular form. A Three Diameter via or a 1-3D via is a through hole having two component dimensions were one is the major dimension of 1-3D length and the other minor dimension is its breadth having a 1D diameter. Finally, a micro milled trench forming a co-axialised structure is used for noise protection EMI protection and is typically elongated longer than 3 times the diameter of the standard circular Micro-via.

Brief Description of the Drawings

The advantages of this invention will be better understood by referring to the accompanying drawing, in which **Fig. 1** shows a top view of a typical profile of power micro-via forming a cross along with a conventional via. **Fig. 2** shows the definition of the length and width of a via in a top exterior view using a cross or "+" shaped via. **Fig. 3** shows an alternate Profile-1 forming an elbow or "L" shaped via. **Fig. 4** shows an alternate Profile-2 forming a "U"

shaped micro via. **Fig. 5** shows an alternate Profile-3 forming a double cross micro via that is not based on the round circular format or were the shape is not centered on the circumference or pitch of the circle diameter. **Fig. 6** shows an alternate Profile-4 forming an "E" shaped micro via that is not based on the round circular format or were the shape is not centered on the circumference or pitch of the circle diameter. **Fig. 7 and Fig. 8** shows the Manhattan Interconnect Strategy. **Fig. 9 and Fig. 10** shows an alternate guard trench. **Fig. 11 and Fig. 12** shows a double guard trench.

Best Mode of Carrying Out the Invention

The inventor has discovered that non-circular vias are feasible for printed circuit boards and are desirable for many reasons. For example a non-circular via can take on an "L" shaped cross section to connect two circuit trace lands or terminal pads on separate circuit board layers while avoiding traces within the region between the legs of the "L" shaped via on layers there between. Other non-circular vias may be used in different ways to adapt to the specific circuit trace layout. It is also desirable to design Vias that are non-circular but are of equivalent overall diameter to comparable standard circular vias because they require less cutting area. This is because, the circumference of a circle is less than some shapes with equivalent overall diameter. The increased circumference makes utilization of non-circular vias

beneficial because the increased circumference of no-circular vias increases the current carrying capacity of the via.

In addition it is found that plated through hole methods can be adapted to be utilized to create a perimeter ground plane trench or an outer shield trench , by using a micro milled trench around the perimeter of a PCB or the perimeter surrounding a component or a set of components and can provide an adequate grounding path for ground traces on multiple layers of the PCB and for multiple components positioned at various locations on the PCB or can be utilized for EMI protection. This technique is useful to conform with the available space of densely populated PCBs and uniquely shaped PCBs. The plated trench can extend through several PCB layers and can follow along the board edge regardless of the shape of the board. The trench structure can also encircle a certain area of the printed circuit board for EMI protection of that specific area of the board or a specific component. The trench provides EMI protection because it creates a coaxialised track structure. If a single trench is used it forms a partial outer shield for the coaxialised structure. The partial outer shield of he coaxialised structure comprises the plating of the wall of the trench, the ground plane, and the plating lip that laterally extends from the rim about the opening of the trench. The plating wraps around the rim of the opening of the trench and laterally extends from the opening forming a lip. The coaxialised structure is completed by the circuit trace co-axially extending through the outer shield formed by the trench.

Current grounding schemes may dedicate entire layers to a grounding plane which unnecessarily increases the thickness and weight of the Board and such a grounding layer usually requires isolation on either side by insulation layers. Another method is to utilize a grounding strip or grounding bar bonded between layers of PCBs or Bonded to the edge of a PCB. This requires a much more difficult manufacturing process and the grounding strip is more difficult to make it accessible to all the circuit traces on all of the layers of the PCB.

In summary, alternative shape features will alter the performance of a micro via by increasing it over known shape (round) performance, for example convoluted or square shaped vias. Three ideas form the basis of what is collectively known as Micro Features, for this invention. These three ideas are categorized as Profile Power Micro via, 1D-3D Vias and the Guard Trench and will now be discussed.

Profile Power Micro via

The basic difference in performance for this alternate micro via, is that it has a greater current carrying capacity than the traditional round or circular micro via of equivalent maximum diametric dimension. As the current carrying capacity of any via is dependent on the circumference wall length and the conducting medium wall thickness, it follows that a larger via (hole) will have a

larger or longer circumference than a smaller counterpart. It is therefore the conclusion that the larger circumference (assuming the same conductive medium thickness) will have a greater amount of conducting medium in which to carry current. Profile Power micro vias for the purposes of this patent application are vias that have a circumference or via edge that is longer or larger than can be obtained by using a "round or circular" shape of equivalent maximum diameter in the design, imaging or manufacturing of micro vias. When used for regular interconnect via creation the shape of the via has as its major dimension the equivalent diameter of the normal circular micro via.

When used for a pure "Power configuration" the normal via max dimension need not apply. In this way the vias can be used in all power and interconnect strategies in PCB design and manufacture. The following are a few examples of the usage of the vias in a power interconnect strategy unrestricted by size constraints.

The Profile Power micro via can be any via that has any shape other than round or circular to create the increased length in circumference over equal diameter circular vias. The shape can for example be star, cross, square or any irregular or convoluted shape that increases the length of the circumference over a round or circular format. In principle the Profile Power micro vias are based on a circular format in that they can have a wave form shape centered on the circumference or pitch circle diameter, however the

power micro via can be an irregular shape that is not based on the round or circular format. That is, the shape of the micro-via cross section can have an irregular shape that is not based on a round circumferencial maximum diameter or circular form. The micro-via can also be a convoluted stepped square pattern.

Also, the non-circular shape can allow more traces on a given layer to connect to a single via in order to connect to traces on other layers. This is possible due to increased current carrying capacity at a given layer because of the increased circumference thereby increasing the number of possible points of interconnection. In addition noncircular vias allow traces and components to be avoided more readily. Another important feature is removal of the inductance characteristic as seen with the standard circular profile via design by eliminating the coil aspect inherent with circular profile vias. Elimination of inductance results in faster signal performance for high-speed signals because the inductance characteristic of the standard circular profile vias has the tendency to slow down a signal. Also, better noise susceptibility performance results from a non-circular format.

1D-3D Vias

The 1D-3D via is an alternate form of the power profile micro via. If the standard or normal "round" micro via is considered as a 1D via or a via with a diameter of the ratio 1.0, then the vias mentioned here are all via

configurations that use a single diameter as the base dimensioning for a via of two component dimensions. Referring to Figure - 2 one of the dimensions is the length 202 and the other is the breadth or width 200. The length can be in the X or Y orientation or any orientation on a two dimensional plane. The same applies for the breadth. Therefore, a via having a round or circular shape ratio of 1.0 : 1.0 is to be considered a normal micro via and is not subject to this patent application.

The benefits to the 1D – 3D shape via configuration are that it can be directional, using the breadth (the smaller dimension) as the limiting factor for interconnect density. The length is restricted to 3D or three times the length of the breadth for this patent application. Vias with a ratio of greater than 3D are considered as "Trenching" and is described in the next section. Use of the 2D and 3D vias being used in a Manhattan configuration is possible, refer to Figs – 7 and 8. This enables a via of sufficient size (current carrying capacity) to be placed within a circuit trace track without round pads. Round vias and hence round via pads are limiting factors in interconnect density in PCB design. If we can use this format in design to realize high density interconnect with the same or increased current carrying capacity as normal vias, then an advantage over normal micro via design and manufacture is attained. As a benefit to the manufacture of PCB's the following can be achieved at the photo resist stage. Photo resist requires a certain minimum area of resist to adhere to the copper surface. During the manufacture of

micro via PCB's the small vias are imaged using a small area of resist. If we assume that normal micro vias have a ratio of 1.0 : 1.0, then we can assume that any via of a greater ratio than 1.0 in one of the two dimensions will have a greater area of photo resist to adhere to the copper or other conductive imageable medium, thereby improving yield.

Trenching

The micro milled trenched is a third form for using the micro via concept of having a non-circular or round cross section. Trenching is a slot that is "micro milled" using plasma or laser processing or other method if removing away material about a centerline. This slot is greater in depth than one layer. Trenching is similar to the 1D-3D via formats shown previously. The difference between 1D/3D vias and trenching is length, the vias with a larger ratio than 3.0 : 1.0 is for this patent called trenching. This does not mean that the two are not interchangeable. There will be instances where the trenching could possibly be smaller that a ratio of 3D, so this must be taken into consideration for this invention. Trenching can be used for EMC screening but this technique can be used for all known reference plane or screening techniques that control signal integrity in laminate interconnect solutions. This trenching can be used on the edge of PCB's or within the area of the PCB. Trenching can be used in all PCB or application specific module types. It offers significant signal performance increases, but at a potentially lower layer count and hence lower production costs.

The premise and the details of the various aspects of the invention can be better understood by referring specifically to the drawing. First, referring to Fig. 1, a power profile non-circular cross section micro via 102 can be seen compared to a standard prior art round or circular cross section micro via 104. The maximum or major diameter 100 for the non-circular or "cross" shaped micro via is equivalent to the standard prior art circular via. This is descriptive of a non-circular micro via having a wave form shape centered on the circumference or pitch circle diameter. It can also be seen that the circumference of the "cross" or "+" shaped micro via is longer than the circumference of the standard circular shaped micro via thereby increasing the current carrying capacity of the via as previously explained. Referring to Fig. 2 the cross-shaped micro via is seen again. What is defined as the width 200 and the length 202 of the micro via is shown. The width 200 of the micro via is driven by the breadth of the cutting action of the cutting means and the length 202 of the micro via is driven by the translation distance of the cutting means. The second length 204 defined as the translation distance of the centerline of the cutting means about which it cuts.

Referring to Figs. 3 and 4, an "L" shaped and a "U" shaped micro via are shown respectively. These alternative cross sections are also based on the round or circular format. However, referring to Figs. 5 and 6, a "double cross" or "++" and an "E" shaped micro via are shown respectively and they

are not based on the round or circular format in that the have a major diameter, 500 and 600 respectively, and a smaller length minor diameter 502 and 602.

Finally, Fig. 6A shows a square micro via having a breadth 604 equivalent to the diameter of a standard circular profile micro via shown as major diameter 100 in Fig. 1.

Referring to Fig. 7, the 1D-3D micro via format as discussed earlier is shown. The 1D micro via 700 is representative of a standard micro via having a circular cross section. The 2D micro via 702 has a minor diameter of breadth 704 and a greater length major diameter 706 where the major diameter is two times the diameter of the minor diameter. The 3D micro via 708 has a minor diameter 710 and a greater length major diameter 712 where the major diameter is three times the diameter of the minor diameter. A means of utilizing the 2D-3D micro via format can be seen by referring to Fig. 8 which shows the "Manhattan" (high density or high population) interconnect strategy 800. One of the benefits of 2D-3D shaped via is that it can be directional, using the breadth (the minor diameter) as the limiting factor for interconnect density. Utilizing the 2D-3D via as part of the Manhattan strategy enables a via of sufficient size (circumference or current carrying capacity) to be placed within a higher resolution (more closely spaced) circuit trace pattern without a round terminal pad or interconnect land. Round terminal pads and round vias can limit trace and interconnect density. If the Manhattan configuration is

used in design to realize a higher density interconnect with the same or increased current carrying capacity, then an advantage over normal micro via design and manufacturer is attained. A second embodiment 802 of the Manhattan strategy 802 is shown where the circuit trace slightly widens to conform to the form of the via to allow greater current carrying capacity in the via.

Referring to Figs. 9 - 11, a novel guard trenching method is shown. Fig. 9 shows a top view of a corner section of a printed circuit board 900 where a plated trench 902 is shown extended about the perimeter of the board. In this preferred embodiment the trenched via is actually one elongated trenched via aligned along the board edge, however the trench could be a series of aligned trench segments (not shown). Also this example shows an EMC sensitive track 904 (a circuit trace that may be EMI susceptible) that extends inside the perimeter and a partial outer shield defined by the trench and extends in parallel to said trench. The trace 904 is shown as segmented because it is hidden; however, the trace is continuous. This inner EMC sensitive track (EMI sensitive circuit trace) completes a coaxial shielding scheme as well as the possibility of a grounding path established by the plated trench. The plated trench via is created by milling a series of elongated trenched through holes along the desired perimeter that extends to and exposes a grounding plane 1000 (Ref. to Fig. 10). The grounding plane 1000, however could be any reference plane fixed at a given potential level. For the embodiment shown in

Fig. 10 the reference plane potential level is fixed at ground. Also note that the ground potential level could be a TTL Logic ground or some other signal ground, chassis ground or some other reference ground. The trench perimeter is preferably a continuous trench. The interior walls 1002 of the elongated through holes and the edges 1004 about the mouth of the holes are then plated with a continuous layer of conductive material 1006 there through thereby providing a path to ground. The structure of the guard trench comprises a micro-milled trench that is plated there through 902. The plating of the trench is continuous along the interior wall 1002 of the trench an extending to the ground plane 1000. The plating wraps around the rim of the opening of the trench and laterally extends from the opening along the edge 1004 about the mouth or opening of the trench forming a lip 1008. The ground plane 1000 and the plating over the interior wall 1002 and the plating lip 1008 form a partial coaxial outer shield about the EMC sensitive inner conductor track 904 thereby creating a coaxial shielding structure.

Referring to Fig. 11 and Fig. 12, double guard trenching 1200 with a coaxialised EMC sensitive track is shown. This is a variation of the above-described guard trenching. This embodiment comprises an inner 1100 and outer 1102 trenched via with a coaxialised EMC sensitive track 1104 (circuit trace) there between. The trace is shown as segmented because it is hidden from view; however, the trace is actually continuous. This embodiment can be exactly the same as the single guard trenching described above with the

exception of having the inner trench for further shielding and to completely surrounding the EMC sensitive track. The double guard trenching provides a continuous and complete outer shield surrounding the EMC sensitive track because of the joining lip structure 1201 of the double trenches.

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What is claimed is:

1. A wiring connection structure for a printed circuit board for interconnecting wiring circuit traces on a plurality of circuit trace layers applied on a plurality of printed circuit board layers and electrically isolated there between by the printed circuit board layers and having a printed circuit board multi-layer structure, characterized by:

a through hole with a convoluted shaped cross section having an interior wall that vertically extends through and intersects and exposes a plurality of wire circuit traces and having a plating of conductive material applied to the interior wall electrically connecting a plurality of wire exposed circuit traces on a plurality of circuit layers.

2. An EMI shielding structure for a printed circuit board for shielding wiring circuit traces on a plurality of circuit trace layers applied on a plurality of printed circuit board layers and electrically isolated there between by the printed circuit board layers and having a printed circuit board multi-layer structure, characterized by:

a trench having a rim about an opening of the trench at a top printed circuit board layer and said trench extending through a plurality of printed circuit board layers to a grounding plane exposing said grounding plane and said trench having an interior wall with a conductive plating

material applied over said wall and said trench having a length greater than two times a breadth of said trench and said wall vertically extends around the perimeter of the printed circuit board and said plating electrically connects to said exposed ground plane and wraps over and laterally extends from said rim forming a lip.

3. A wiring connection structure for a printed circuit board for interconnecting a plurality of wiring traces applied on a plurality of printed circuit board layers and electrically isolated by printed circuit board layers and having a printed circuit board first layer with a main surface, characterized by:

a first wire trace applied to said main surface having a first terminal landing pad with a first through hole there through, said first through-hole having a convoluted shaped cross section with a continuous perimeter;

a printed circuit board first insulation layer formed over said first wire trace having a second through hole of identical cross sectional geometry to and vertically aligned with the first through hole and extending to the first terminal landing pad exposing a portion of said first landing pad; and

a second wire trace applied to the printed circuit board first

insulation layer having a second terminal landing pad with a third through hole having identical geometry to and vertically aligned with the first and second through holes, wherein said first, second and third through holes are adjoining and are plated there through with an electrically conductive material forming a plated through hole with a convoluted cross section that vertically intersects the first and second terminal pads and electrically connects the first wire trace and the second wire trace by a connection between the first and second wire trace terminal landing pads and the plated through hole.

4. The wiring connection structure of **claim 3**, wherein the first through hole has a shaped continuous curved cross section centered on a circumference diameter of a standard single diameter circular profile micro via and wholly contained within a perimeter defined by the circumference diameter.

5. The wiring connection structure of **claim 4**, wherein the continuous curved cross section is "U" shaped.

6. The wiring connection of **claim 4**, wherein the continuous curved cross section is "L" shaped.

7. The wiring connection of **claim 4**, wherein the continuous curved cross section is "+" shaped.

8. The wiring connection structure of **claim 3**, wherein the first through hole has a shaped continuous curved cross section centered on a circumference diameter of a standard single diameter circular profile micro via and extends beyond the perimeter defined by the circumference diameter.

9. A reference plane structure of a printed circuit board for fixing a potential reference for a plurality of wiring circuit trace layers that are electrically isolated there between by a plurality of printed circuit board layers and having a printed circuit board first layer with a main surface, characterized by:

a first wire trace circuit layer applied to said main surface;

a first printed circuit board-insulating layer formed over said first wire trace circuit layer;

a first reference plane applied over the first printed circuit board insulation layer;

a trench having an interior wall and extending about a perimeter encompassing the first wire trace circuit layer and extending through the printed circuit board first layer, extending through and exposing the first wire trace circuit

layer, extending through the first insulation layer and extending to the reference plane exposing said reference plane; and

a conductive plating layer on the interior wall electrically connecting the first wire trace layer to the grounding plane.

10. The reference plane structure of **claim 9,** where the perimeter encompasses a portion of the first wire trace circuit layer.

11. The reference plane structure of **claim 9**, where the reference plane is fixed at a ground potential.

12. The reference plane structure of **claim 9**, where the reference plane is fixed at a reference voltage.

13. A wiring connection structure for a printed circuit board for interconnecting a plurality of wiring circuit traces applied on a plurality of printed circuit board layers and electrically isolated by printed circuit board layers and having a first printed circuit board layer with a main surface, characterized by:

a first wire circuit trace having a width applied to said main surface and having a first terminal landing pad with a terminal width the same as the width of the first wire trace

and having a first through hole with a major and minor diameter where the minor diameter is less than the width of the first trace and the major diameter is elongated and directional along a direction of the terminal landing pad;

a printed circuit board first insulation layer formed over said first wire trace having a second through hole having identical geometry and orientation as and vertically aligned with the first through hole and extending to the first wire trace terminal landing pad; and

a second wire circuit trace applied to the printed circuit board first insulation layer having a second terminal landing pad with a third through hole having identical geometry to and aligned with the first through hole,

wherein said first, second and third through holes are adjoining and are plated there through with an electrically conductive material forming a plated through hole vertically intersecting the first and second terminal pads and electrically connecting the first wire trace and the second wire trace by a connection between the first and second landing pads and the through hole.

14. The wiring connection structure of **claim 13**, wherein the major diameter is at least about twice that of the minor diameter.

15. The wiring connection structure of **claim 13**, wherein the major diameter is at least about three times that of the minor diameter.

16. A wiring connection structure for a printed circuit board for interconnecting a plurality of wiring circuit traces applied on a plurality of printed circuit board layers and electrically isolated by printed circuit board layers and having a first printed circuit board layer with a main surface, characterized by:

a first wire circuit trace having a first width applied to said main surface and having a first terminal landing pad with a second width which is greater than the first width and having a first through hole with a major and minor diameter and the minor diameter is less than the second width and the major diameter is greater than the first width and is directed along and within the terminal landing pad;

a printed circuit board first insulation layer formed over said first wire trace having a second through hole of identical geometry and orientation as and vertically aligned with the first through hole and extending to the first wire trace terminal landing pad; and

a second wire circuit trace applied to the printed circuit board first

insulation layer having a second terminal landing pad with a third through hole having identical geometry to and aligned with the first through hole,

wherein said first, second and third through holes are adjoining and are plated with an electrically conductive material forming a plated through hole vertically intersecting the first and second terminal pads and electrically connecting the first wire trace and the second wire trace by a connection between the first and second landing pads and the through hole.

17. A method of interconnecting a plurality of wiring circuit traces applied on a plurality of printed circuit board layers and electrically isolated by printed circuit board layers characterized by the steps of:

applying a first wire trace to a main surface of a first printed circuit board layer where said wire trace has a first terminal landing pad;

forming a first printed circuit board insulation layer over said first wire trace;

applying a second wire trace over the first insulation layer, said trace having a second terminal landing pad vertically aligned over the first landing pad;

cutting with a cutting means vertically down through the first

landing pad, the insulation layer, and the second landing pad removing away material about an axial centerline of the cutting means with a generally circular patterned cutting action;

translating the cutting means laterally while continuing the circular patterned cutting action forming a non-circular through hole through the first and second pads and the insulation layer to define an interior wall and exposing the first and second terminal pads; and

plating the interior wall with an electrically conductive material, electrically connecting the first and second wire traces by the connection established between the first and second terminal landing pads and the electrically conductive material plating.

18. The method of interconnecting a plurality of wire traces of **claim 17,** the cutting is cutting by plasma ablation.

19. The method of interconnecting a plurality of wire traces of **claim 17,** the cutting is cutting with a laser.

20. A method of grounding and shielding a plurality of wiring circuit traces applied on a plurality of printed circuit board layers electrically isolated

by a plurality of printed circuit board layers characterized by the steps of:

applying a first wire circuit trace to a main surface of a first printed circuit board layer said first wire trace having a first ground terminal lead;

forming a first printed circuit board insulation layer over said first wire trace;

applying a grounding plane over the first printed circuit board insulation layer;

cutting vertically down through the first printed circuit board layer and the first insulation layer removing away material about an axial center line with a generally circular patterned cutting action with a cutting means to a depth sufficient to transcend the first wire trace and extend to the grounding plane ;

translating the cutting means laterally while continuing the circular patterned cutting action forming a trench extending to form a perimeter at least partially about the first wire trace having an interior wall exposing the first ground terminal lead and the ground plane; and

plating the interior wall of the trenched through hole with an electrically conductive material electrically connecting the first trace to the grounding plane.

21. An EMI shielding structure for a printed circuit for shielding a plurality of wire circuit trace layers that are electrically isolated by printed circuit board layers, characterized by:

a printed circuit board having a plurality of wire trace circuit layers and a plurality of printed circuit board insulation layers there between and having a plurality of printed circuit board edges and a grounding plane; and

a first trench having an interior wall and extending in parallel with the board edge within a perimeter defined by the board edge encompassing the printed circuit board wire circuit trace and extending through the printed circuit board layers and extending to the ground plane, exposing said ground plane; and

an electrically conductive plating material applied over the interior wall there through and electrically connecting to the exposed ground plane providing at least a partial perimeter shield for the printed circuit board.

22. The EMI shielding structure of **claim 21,** where the perimeter encompasses a portion of the printed circuit board.

23. The EMI shielding structure of **claim 21**, further characterized by:

a second trench having an interior wall and extending wholly within and in parallel with an outer perimeter defined by the first trench and extending through the printed circuit board layers and extending to the ground plane exposing said ground plane,

wherein the second trench interior wall is plated with an electrically conductive plating material applied over the interior wall there through and electrically connecting to the exposed ground plane providing a double trench shield.

24. The EMI shielding structure of **claim 21**, further characterized by:

an EMC sensitive track of conductive material extending wholly within and parallel with an outer perimeter defined by the first elongated through-hole and disposed between circuit board insulation layers through which the trenched through-hole extends.

25. An EMI shielding structure for a printed circuit for shielding a plurality of wire trace layers that are electrically isolated by printed circuit board layers characterized by:

a printed circuit board having a plurality of wire trace circuit

layers and a plurality of printed circuit board insulation layers there between and having a grounding plane layer with all layers bonded one over another;

a first trench with an continuous rim about an opening of the trench at a top layer of the printed circuit board and said trench having an interior wall and said trench extending around a perimeter of the printed circuit board;

an electrically conductive plating applied over the interior wall of the trench extending and electrically connecting to the ground plane and extending to an wrapping over the rim and extending laterally from said rim forming a lip; and

an EMC sensitive track coaxially extending through a partial outer shield defined by the trench interior wall, the plating lip and the ground plane.

26. The EMI shielding structure of **claim 25**, further characterized by:

a second trench with an continuous rim about an opening of the trench at a top layer of the printed circuit board and said trench having an interior wall and said trench extending in parallel with the first trench around a perimeter within the first trench; and

an electrically conductive plating applied over the interior wall of

the trench extending and electrically connecting to the ground plane and extending to an wrapping over the rim and extending laterally from said rim forming a second lip which joins the first lip,

where the EMC sensitive track coaxially extends through an outer shield defined by the first and second trench interior walls, the first and second plating lips and the ground plane.

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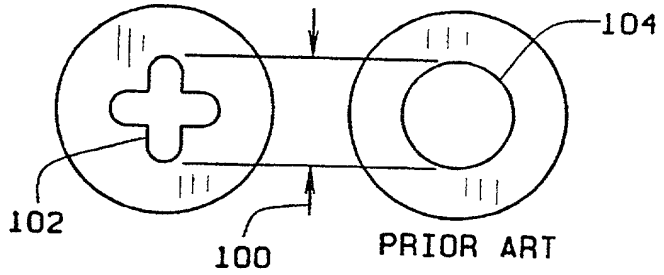

FIG. 1

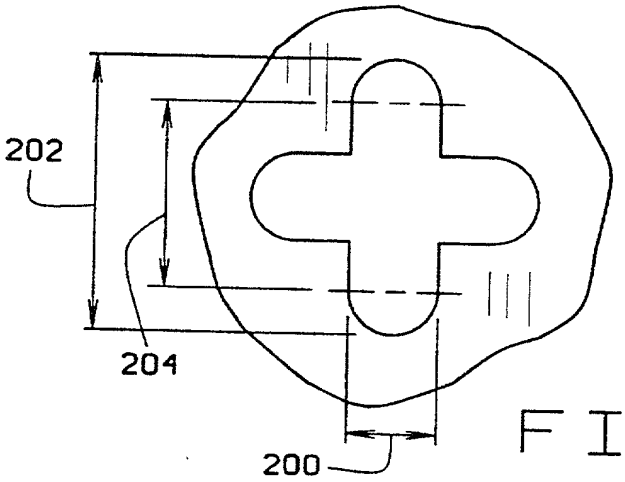

FIG. 2

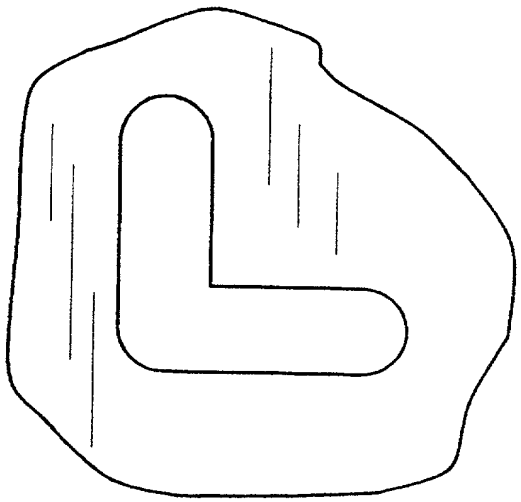

FIG. 3

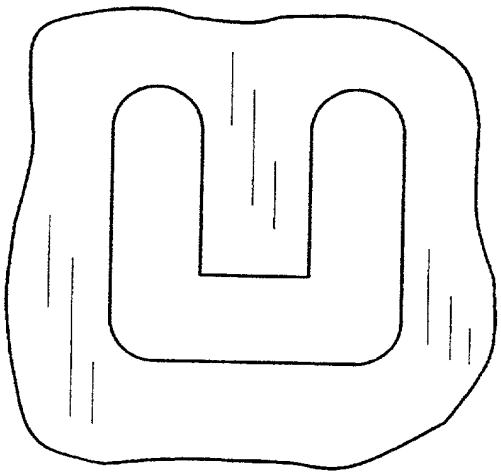

FIG. 4

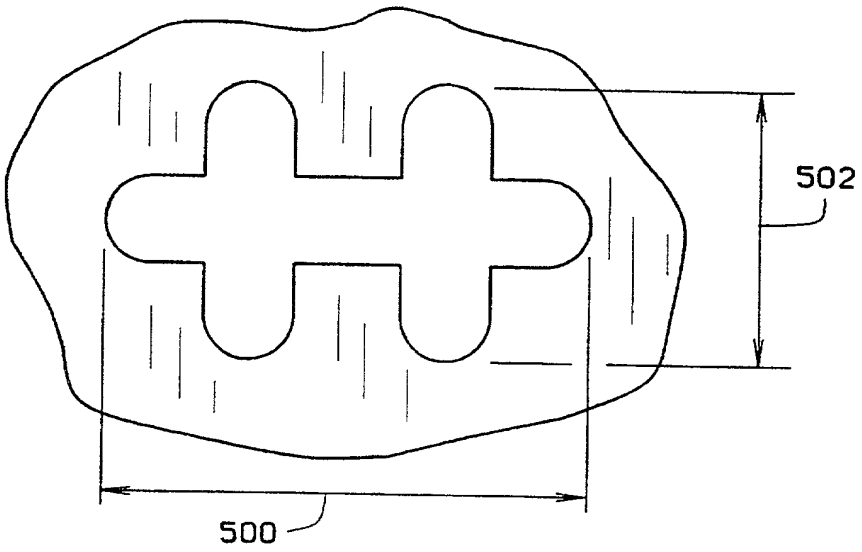

FIG. 5

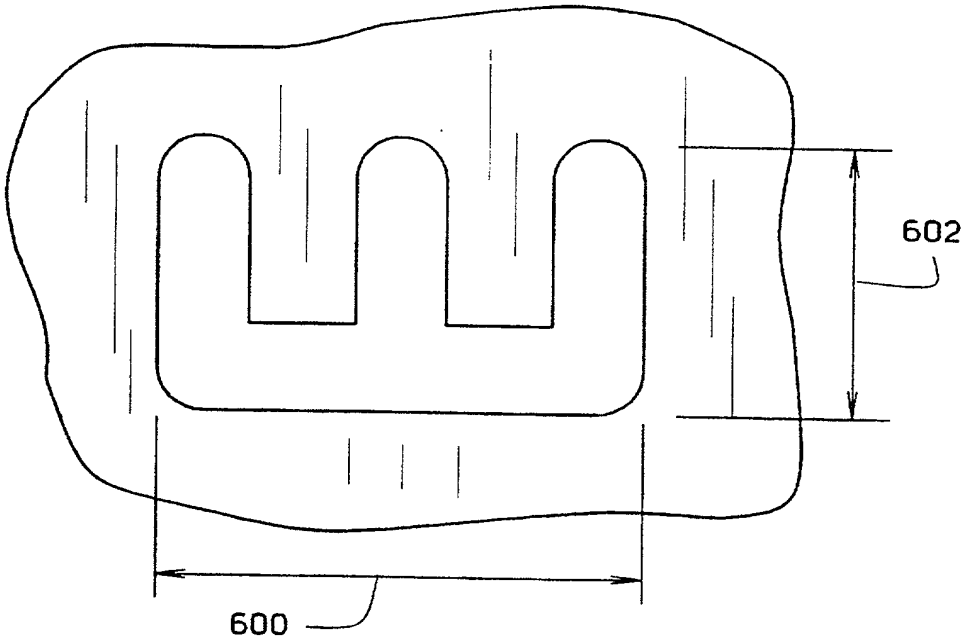

FIG. 6

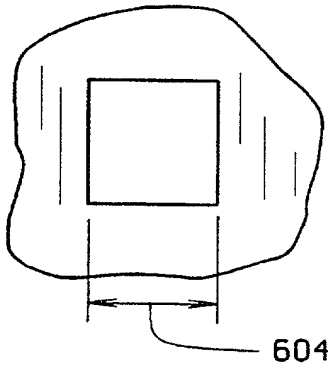

FIG. 6A

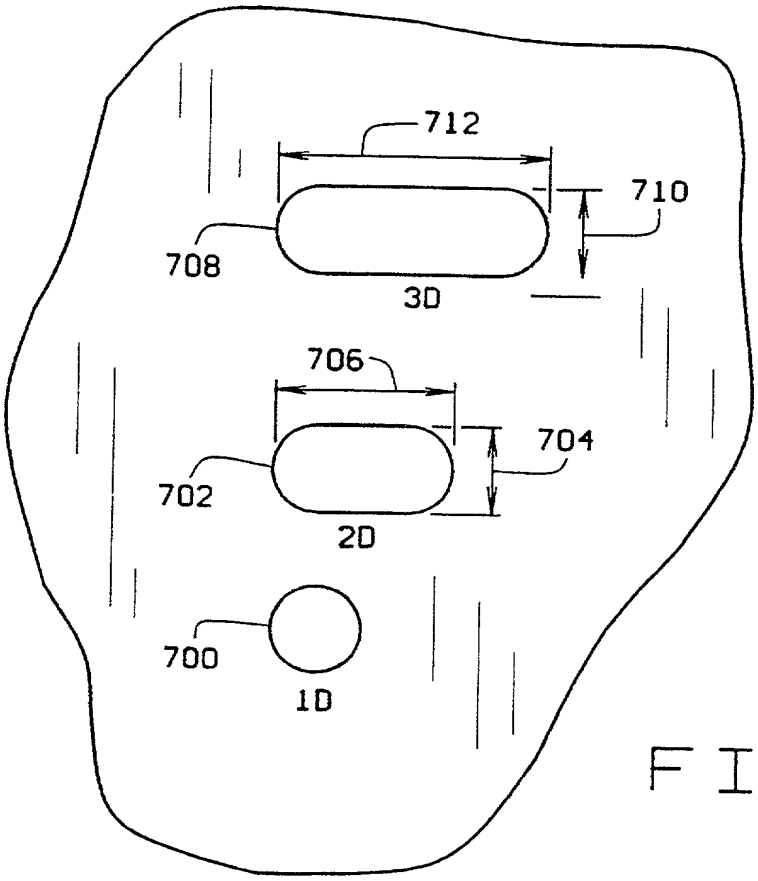

FIG. 7

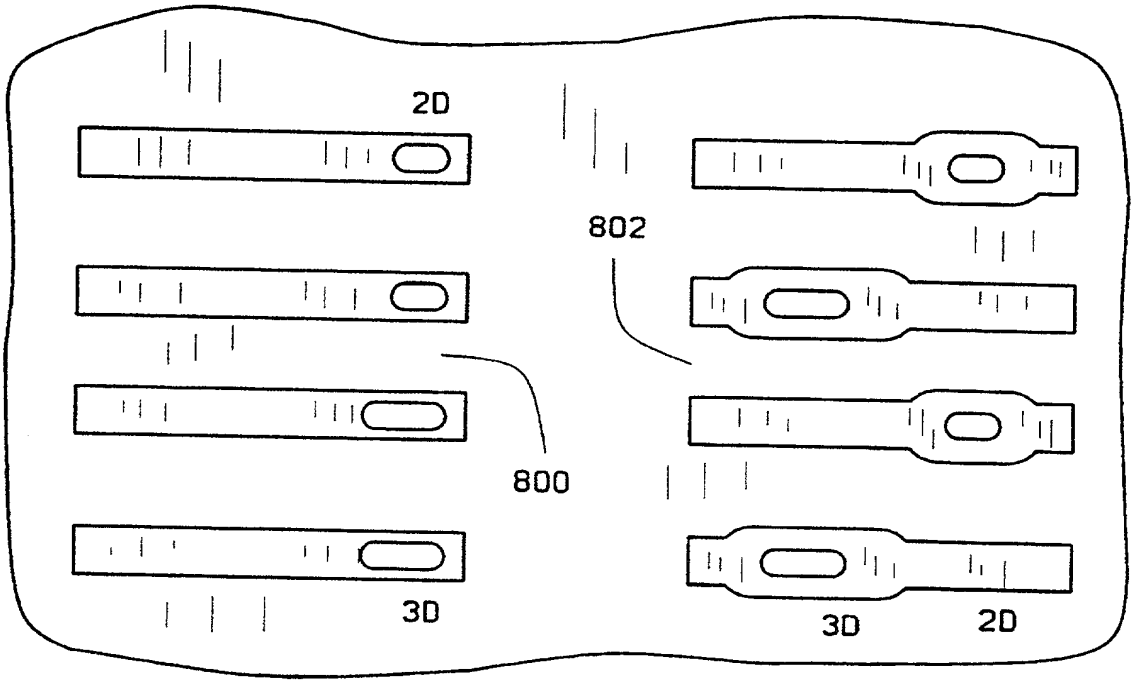

FIG. 8

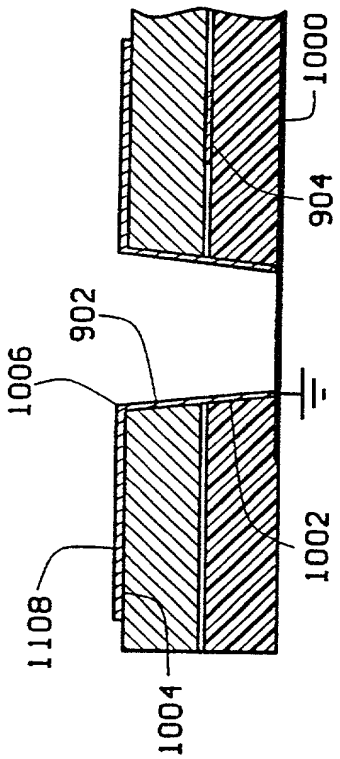

FIG. 10

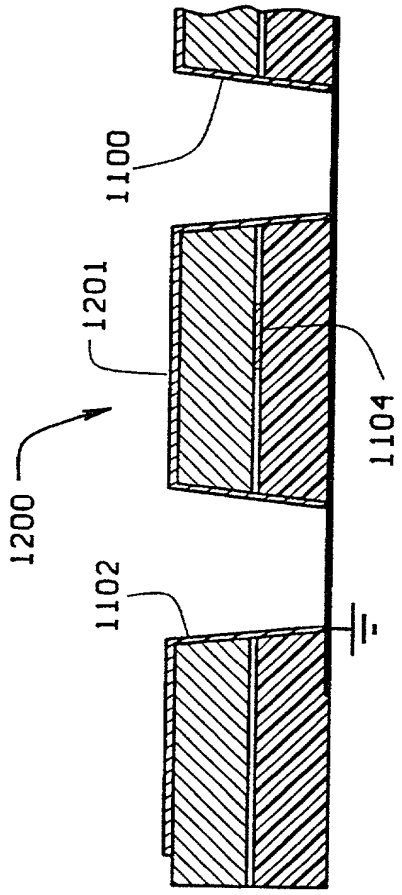

FIG. 12

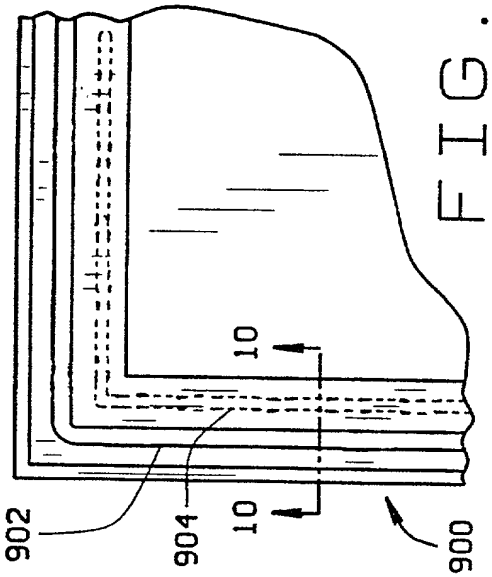

FIG. 9

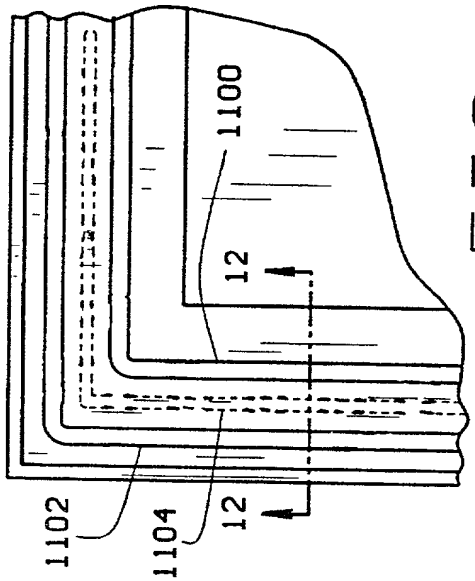

FIG. 11

Docket No. 2654-005US #3

Declaration For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

the specification of which

(check one)

☐ is attached hereto.

☒ was filed on March 9, 2001 as United States Application No. or PCT International Application Number 09/786,787

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

60/099,730	10 September 1998
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, CFR Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

PCT/US99/20418	7 September 1999	Pending
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor **Martin A. Cotton**
Sole or first inventor's signature MCott Date 11-6-01
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Third inventor's signature Date
Residence
Citizenship
Post Office Address

Full name of fourth inventor, if any
Fourth inventor's signature Date
Residence
Citizenship
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